Report No. 280

ILLINET ANALOG FACILITIES

September 5, 1968

DEPARTMENT OF COMPUTER SCIENCE · UNIVERSITY OF ILLINOIS · URBANA, ILLINO

Report No. 280

ILLINET ANALOG FACILITIES

by

R. A. Wells
C. E. Carter
H. G. Friedman

September 5, 1968

Department of Computer Science
University of Illinois
Urbana, Illinois 61801

CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABSTRACT

The Department of Computer Science has installed an IBM 1800 computer at the Digital Computer Laboratory. The 1800 is a medium-speed digital computer which has the special capability of analog-digital data conversion to and from a variety of storage media. It is especially suitable for the direct acquisition of data from an experiment, with the possibility of feedback to control of the experiment. Since the 1800 is attached to the System/360 complex, data processed by one computer is readily available to the other; for example, in one job a typical analog/digital user might digitize analog data on the 1800 and then process the data with a FORTRAN program on the System/360-75.

1. Introduction

In order to add analog conversion capability to the central facilities of the ILLINET, the Department of Computer Science has attached an IBM 1800 computer to the IBM System/360 complex at the Digital Computer Laboratory. Attachment of the two machines gives the user the full analog, digital, and control input/output capabilities of the 1800, plus the full computational capabilities of the System/360, including the ability to process analog-converted data on the 360-75.

The 1800 is capable of taking input from devices such as audio tape recorders and experimental apparatus of the type which traditionally produces output on polygraphs, teletypewriters, or punched paper tape. It can also output to such devices, and thus has the capability to control the progress of an experiment by feedback from partial data.

This report discusses the hardware and software available on the 1800. The hardware consists, for the most part, of standard IBM 1800 components. However, in order to integrate the 1800 into the ASP system operated on the central System/360, the 1800 software has been designed especially by DCS.

Any job submitted from any ILLINET input device may include steps to be executed on the 1800, as well as steps to be executed on the 360-75. Typically, the user will set up and operate his own equipment attached to the 1800 as his program executes.

This report is preliminary, in that it was written before the software package for the 1800 was complete and before any significant amount of operating experience had been gained with it. More up-to-date material will appear in future editions as the software is developed and operating experience is gained.

2. Hardware

2.1. Summary

The 1800 hardware is diagrammed in Figure 2.1. It includes:

1801 processor-controller (PC)
1054 paper-tape reader
1055 paper-tape punch
1816 printer-keyboard console typewriter
1442 punched-card reader/punch*
1443 line printer*
2310 disk drive
access to 2401 magnetic tape drives
access to 360-50/75 system
analog/digital input
digital/analog output
high speed register output
electronic contact-operate output
contact-sense input
process interrupt input

Figure 2.2 is a more detailed layout of the individual devices and components that make up the system. Table 2.1 identifies these devices by number and name. Table 2.2 presents interrupt and addressing information on the various components of the system.

The 1442 card read/punch and 1443 printer are temporary. The analog to digital converter and multiplexor shown may be replaced by higher-speed non-IBM components at some time in the future.

---

*Temporary

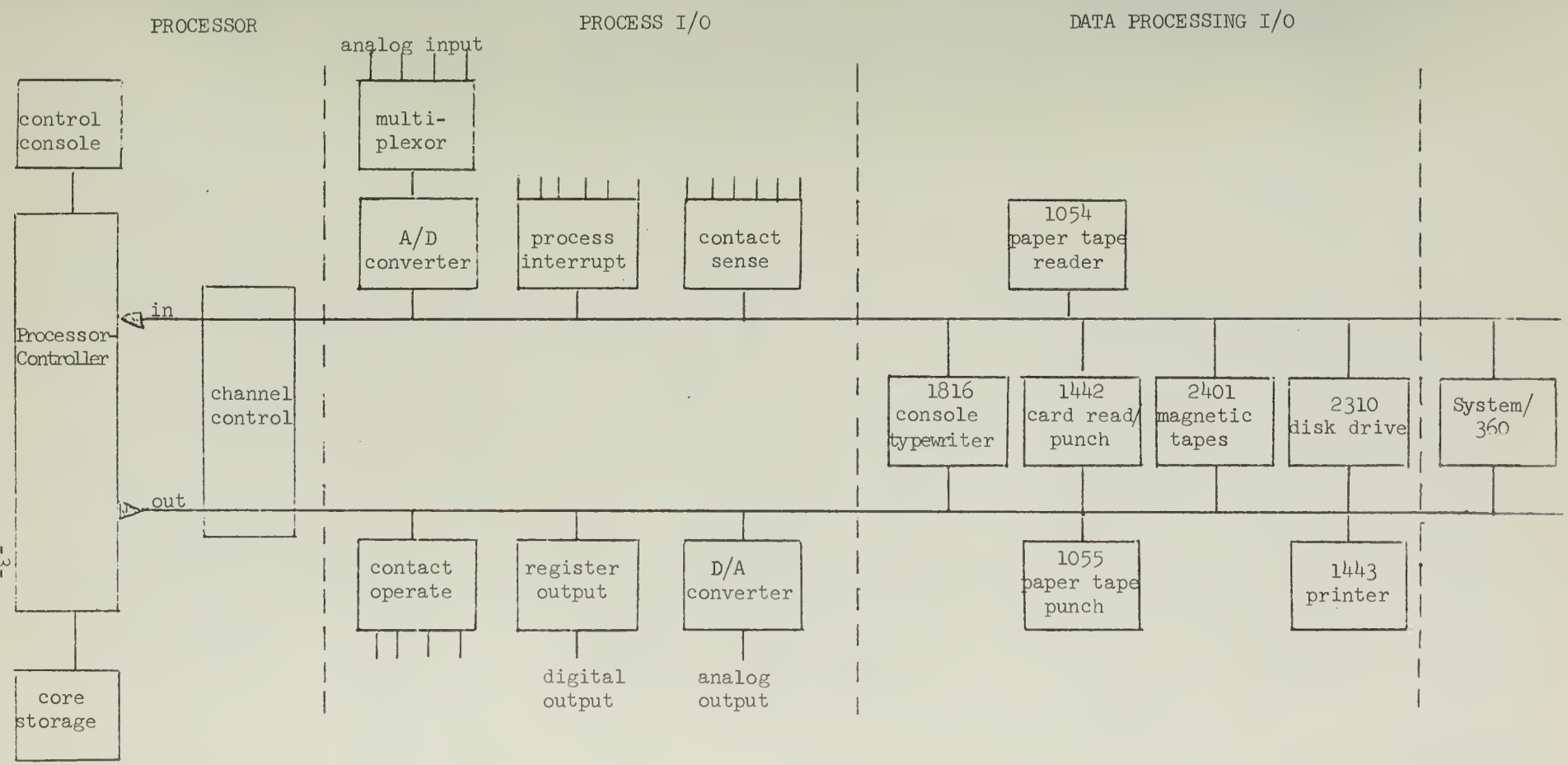


Figure 2.1. General Configuration

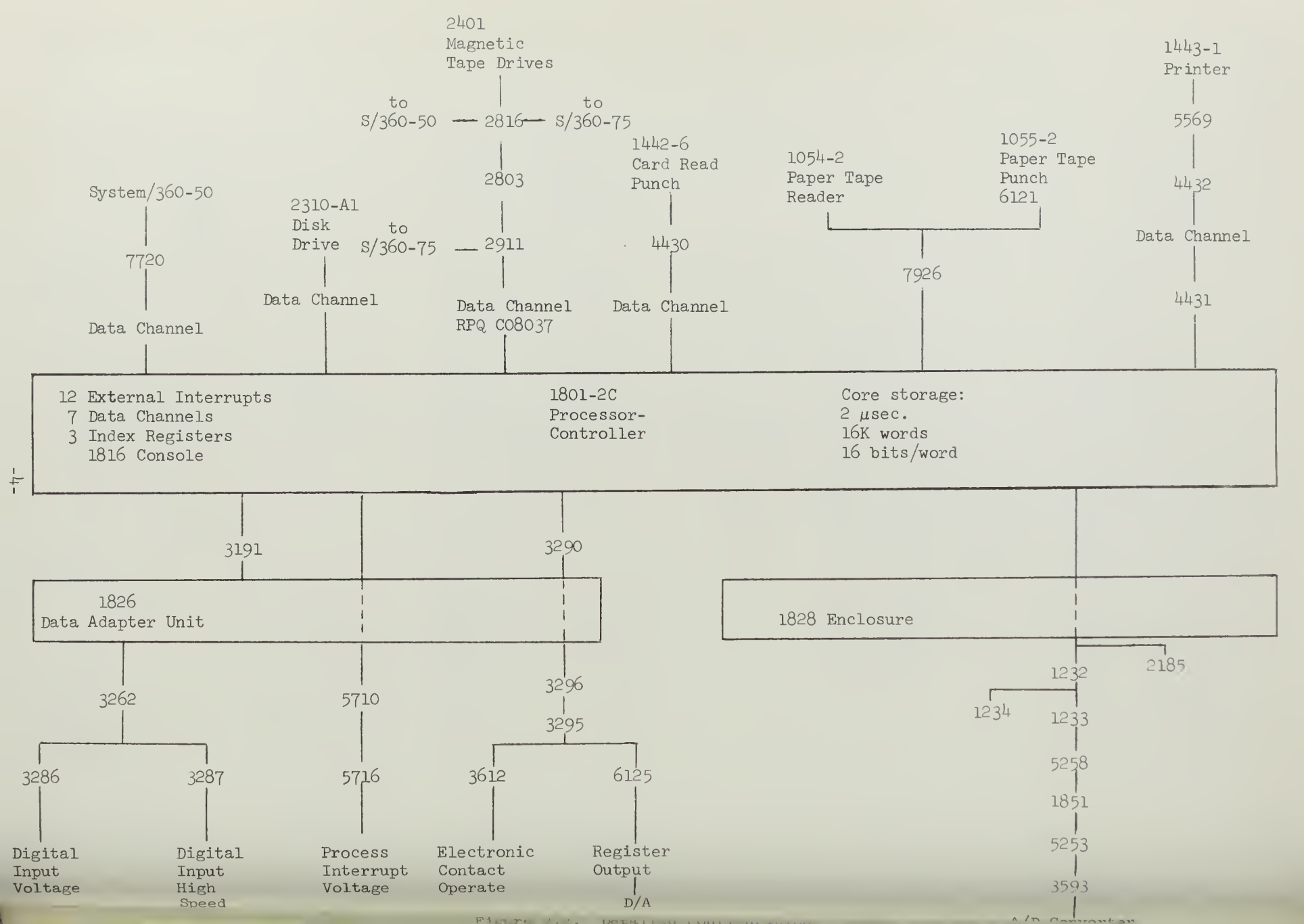

2401
Magnetic
Tape Drives
to
S/360-50
2816
to
S/360-75
1443-1
Printer
5569
4432
Data Channel
4431
1442-6
Card Read
Punch
1054-2
Paper Tape
Reader
1055-2
Paper Tape
Punch
6121
2803
System/360-50
7720
Data Channel
2310-A1
Disk
Drive
Data Channel
to
S/360-75
2911
Data Channel
RPQ C08037
4430
Data Channel
7926
12 External Interrupts
7 Data Channels
3 Index Registers
1816 Console
1801-2C
Processor-
Controller
Core storage:
2 μsec.
16K words
16 bits/word
-4-
3191
3290
1826
Data Adapter Unit
1828 Enclosure
2185
1232
1234
1233
5258
1851
5253
3593
A/D Converter
3262
5710
3296
3295
3286
3287
5716
3612
6125
Digital
Input
Voltage
Digital
Input
High
Speed
Process
Interrupt
Voltage
Electronic
Contact
Operate
Register
Output
D/A

Table 2.1.
Component Identification

1801-2C processor-controller

Memory: 2μsec., 16K words, 16 bits/word

Standard features:

12 External interrupt levels
3 Data channels
3 Index registers
3 Internal timers
Operator's console

1054-2 paper tape reader

1055-2 paper tape punch

1232 analog-digital converter, model 2

1233 analog input data channel

1234 analog input data channel adapter 2

1442-6 card reader/punch, 9247 priority #7

1443-1 printer, 9256 priority #6

1816 console typewriter

1826 data adapter unit

1828 enclosure

1851 multiplexor control

2185 comparator

2310-A1 disk, single module, single platter, 9161 priority #1

2401 magnetic tape drives, 9232 priority #2

2803 magnetic tape control unit (shared with 360-75 via 2911 switch)

2816 switching unit for magnetic tape drives

2911 switching unit for magnetic tape control

3222 four extra data channels

3262 digital input adapter

3286 digital input, voltage sense (one group of 16 bits)

3287 digital input, high speed (one group of 16 bits)

3290 digital channel output adapter, 9275 priority #5

3291 digital channel input adapter, 9284 priority #4

3295 digital output adapter

3296 digital output control

3593 connector element (±5v)

3612 electronic contact operate (16 bits)

4430 reader-punch controller

4431 printer adapter

4432 printer controller

5253 group of 16 points on analog multiplexor

5258 multiplexor control

5569 printer controller

5710 process interrupt adapter

5716 process interrupt, voltage (one group of 16 bits)

6121 take-up reel for paper tape punch

6125 register output, high speed

7720 360 channel adapter, 9743 priority #3

7926 paper tape adapter

9665 internal timer, 0.125 msec.

9681 internal timer, 4.0 msec.

9683 internal timer, 8.0 msec.

RPQ C08037 System/360-type 1800 data channel

Table 2.2.
Interrupt and Addressing Summary
of Input/Output Devices

Device	Interrupt Level	ILSW Bit	Data Channel	Area Code
Process Interrupt	00	00		11
Interval Timers	00	01		
2310 Disk	01	00	1	04
360 Ch. to Ch.	02	00	3	13
Magnetic Tape Drives	03	00	2	18
Typewriter	04	00		01
Comparator	04	01	5	
Digital Input	05	00	6	11
Digital-Analog Output	05	01	7	12
Analog-Digital Input	05	02	4	10
1443 Printer	06	00	8	06
1054/1055 Paper tape read-punch	06	01		03
1442 read-punch	07	00	9	02
Console Interrupt	08	00		

The system includes a single analog-to-digital converter which can receive signals from one or more multiplexor input points, under control of the 1800 program. A sample-and-hold amplifier permits conversion rates up to 20,000 conversions per second. The system can also sense binary conditions, such as the open or closed state of a switch, either under the initiative of the 1800 program (using the contact sense feature) or by interrupt of the program (using the process interrupt feature).

Analog output is accomplished through a fast digital output register, which can be used to drive various output devices. It is expected that a DCS digital-to-analog converter, presently connected to the ILLIAC II, will be connected to the 1800 through this register. The system also has 16 electronic contact operate output points, which can be used to cause any desired program-controlled operation such as turn-on-tape-drive, etc.

The access to the System/360-50 is a channel-to-channel adapter which allows information to be exchanged between the 1800 and the 360-50 in burst mode at selector channel speeds. The access to tape units is through an electro-mechanical switch which allows the 1800 to use the 9-track phase-encoded 180 KHz magnetic tape drives that are a part of the System/360-50/75.

2.2. 1800 Processor

The 1800 is a general purpose digital computer with interrupt and channel capability. The central processing unit is an 1801 model 2C processor-controller, having 16K words of 2 μsec core storage. Each core word has 16 data bits, 1 parity bit, and 1 storage protect bit. The processor is generally applicable to problems in the area of process control or high speed analog data acquisition.

2.3. Data Processing Input/Output

2.3.1. 1054 Paper Tape Reader (model 2)

This tape reader reads one-inch eight-track tape at a maximum rate of 14.8 characters/second. Data is read into core storage as an image of the holes in the tape, with each punched character being read into one addressed core location.

2.3.2. 1055 Paper Tape Punch (model 2)

This tape punch punches one-inch eight-track paper tape at a maximum rate of 14.8 characters/second. Data characters are punched as an image of the data in core storage.

2.3.3. 1442 Card Read/Punch (model 6)

This read/punch operates on a data channel and provides serial reading and punching of cards. The model 6 reads cards at 300 cards/minute and punches cards at 80 columns/second.

2.3.4. 1443 Printer (model 1)

This printer operates on a data channel at a speed of 150 lines/minute, on a 120 character line with a 52 character set: 10 numeric, 26 alphabetic, and +&-/%¤#=,.$@()*'

2.3.5. 1816 Keyboard-Printer

This console typewriter provides printed output at the rate of 14.8 characters/second and a keyboard for data entry into the processor.

2.3.6. 2310 Disk Drive (model A1)

This is a single platter moveable head disk consisting of one drive mechanism. The 2315 cartridge consists of a single platter of 203 cylinders of two tracks each. Each track consist of 4 sectors of 321 words each. One word is stored on disk as 16 data bits plus 1 parity, 1 storage protect, and 2 spacing bits. The maximum storage capacity in a single access is 2568 words.

2.3.7. 2401 Magnetic Tape Drives (model 6)

These drives are phase-encoded 180,000 bytes/second tape drives handling one-half inch tape of the regular 10.5 inch reel, 2400 foot length variety. The capacity of a 2400 foot reel of tape written on this drive is:

20 byte block size-42,847 blocks or 856,940 bytes,
100 byte block size-39,846 blocks or 3,984,600 bytes,
500 byte block size-29,510 blocks or 14,755,000 bytes,
1000 bytes block size-22,284 blocks or 22,284,000 bytes,
2000 byte block size-14,959 blocks or 29,918,000 bytes.

One 1800 word (16 data bits + 1 parity bit) is written on tape as two consecutive bytes (8 data bits + 1 parity bit each).

There are six tape drives shared by the 360-50, the 360-75, and the 1800. Each computer is connected to the tape drives via its data channel and a 2803 control unit. The three 2803 control units are connected through a 2816 switching unit to the tape drives in such a way that all three computers can access all six tape drives. The switching function of the 2816 is done automatically, although the operator can manually disconnect any given tape drive from any given control unit. The 2803 control unit used by the 1800 is also connected, via a 2911 switching unit, to a second channel of the 360-75. The 2911 is a manual switch only. This arrangement allows the 360-75 an alternate path to the tape drives during periods when the 1800 is not using them.

2.3.8. 7720 1800-System/360 Channel-to-Channel Adapter

This is a direct core-to-core connection via a data channel on each of the two computers. Thus, the 1800 and the 360-50 each look like an input/output device to the other. This device is similar to the channel-to-channel adapter which is used to connect the 360-50 to the 360-75.

2.4. Process (Analog, Digital, and Control) Input/Output

2.4.1. Process Interrupt, Voltage

Process interrupt is factory wired to one of 24 priority levels of processor interrupt. When an interrupt occurrs, the processor program will branch to an interrupt routine associated with that level. If a higher level interrupt routine is in progress, the new condition waits until the higher one is completed.

Each pair of customer terminals is factory wired to a particular bit position of a 16-bit Process Interrupt Status Word (PISW). Each PISW is interrogated as a 16-bit word for individual terminal identification by a program.

Sense specifications:

1. Contact Grouping: 16 voltage input group.
2. Transmission Path: Line lengths and resistance may be of any magnitude as long as the dc voltage levels appear within tolerance at the customer terminals.
3. Interrupt Condition: An interrupt will occurr by a voltage level changing from "0" to "1". Interrupt is initiated on the leading edge of the voltage rise.

   Binary "1" = -1.0 vdc min. to +30 vdc max.
   Binary "0" = -6.0 vdc min. to -30 vdc max.
   Indeterminate = -6.0 vdc to -1.0 vdc
4. Input Impedance: 3.7k ohms (approx.)
5. Sensing delay: Filter and line capacitance introduce a delay before the system can reliably detect a change in voltage level. The following maximum delay values are for line lengths up to 250 feet. The capacitance of longer line lengths will increase the delays.

   Voltage level input to reliable detection = 2.5 msec. max.
   Max. "1" voltage to reliable "0" = 5 msec. max.

6. Safety protection: The equipment will tolerate accidental connection to voltage as high as 120 v ac without damage other than the possible opening of the fuse in the dc ground line.
7. Electrical noise protection: The voltage source should be referenced only to the 1800 system ground through the common or dc return lead of the signal wiring. If desired, a single power supply may be used for more than one input when located in the same immediate area.
8. Terminal description: A fanning strip with screw-driver connections is used for customer wires.
9. Circuit description: See Figure 2.3, process interrupt, voltage sense schematic.
10. Wiring practice: Twisted pair wiring is recommended for each individual voltage source. Two wire termination is provided for each source. Terminal sizes are #8 on standard barrier strips. No tiedown for shielding is provided. It is recommended that the customer provide reasonable physical separation from output and analog system wiring and from any ac power lines enroute.

2.4.2. Contact Sense, Voltage

Digital input points may be used either collectively as a 16-bit register input or individually for the sensing of separate process conditions. The input data is read by the processor-controller on command as binary "1" or "0" bits in a 16-bit word. Input data is sensed by a voltage change.

The specifications are the same as process interrupt (see section 2.4.1) with the following exception:

2. Transmission path: limited to 100 ft.

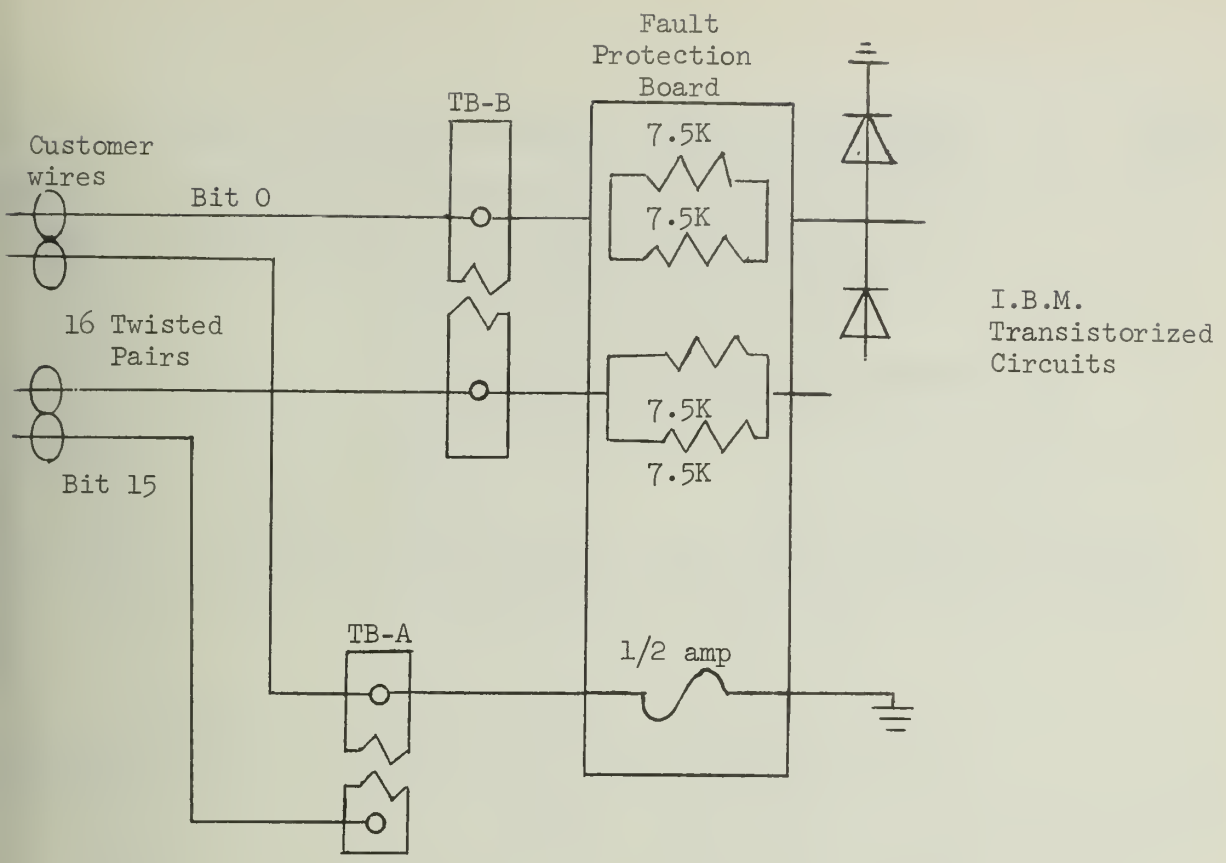


Figure 2.3.
Process Interrupt, Voltage Sense Schematic

2.4.3. Electronic Contact Operate (ECO)

This feature provides program selection of one or more output points (within a group of 16), permitting the closing of customer circuits for a period of time controlled by the program. The specifications governing the customer's input voltage and load characteristics are:

1. Ground: Common or dc return is connected to the 1800 system ground. To avoid ground loops or injection of noise into the system the customer's voltage source should be floating or isolated from ground at the voltage source.
2. Customer Power Supplies: Each power supply furnishes power to four (or multiples of four) digital output points.
3. Load Current (switched): Must not exceed 0.45 amp.

4. Load Characteristics: A wide variety of R, L, and C load characteristics can be accommodated within the above voltage and current specifications provided the peak instantaneous voltage at the terminals does not exceed:

   +65 v dc maximum, +1 v dc minimum

5. Output Impedance: Diode - "1" (on) = 5-7 megohms
   "0" (off) = 8.0 ohms
   Switch - "0" (off) = 1.25 megohms
   "1" (on) = variable

6. Transfer Time (resistive load):

   Less than 10 μsec for turn on.

   Less than 10 μsec for turn off.

7. Duration of Closure: Duration selected by program.

8. Synchronization: Generation of program action may be initiate by an external "sync" signal.

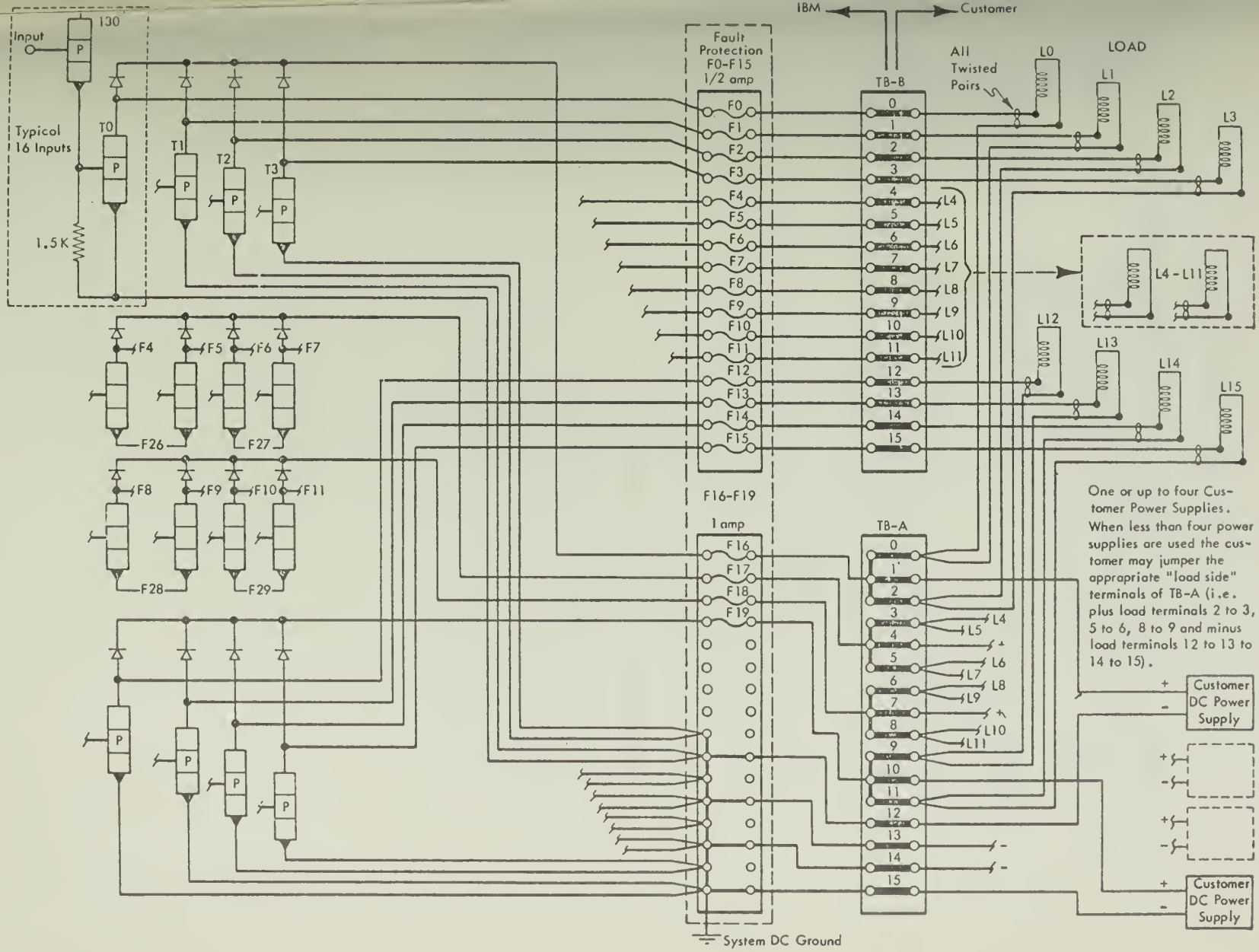
9. Terminal Description: ECO is terminated in the customer access area at the rear of the 1801 processor-controller.

10. Circuit Description: See Figure 2.4.

11. Wiring Practice: Use twisted pair wiring to reduce electrical interference. The electronic contact operate wiring should not be run in the same cable with analog or digital inputs.

2.4.4. Register Output (RO)

Register Output is a 16-bit binary register which can transmit its contents over 16 pairs of conductors to a customer provided device. Transfer of this data is under program control and can be initiated by the customer device (either an external sync signal, or process interru).


IBM
Customer
Input
130
P
Typicol
16 Inputs
T0
T1
T2
T3
1.5K
Fault
Protection
F0-F15
1/2 amp
TB-B
All
Twisted
Poirs
L0
LOAD
L1
L2
L3
F0
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
F13
F14
F15
L4
L5
L6
L7
L8
L9
L10
L11
L4 - L11
L12
L13
L14
L15
F4
F5
F6
F7
F26
F27
F8
F9
F10
F11
F28
F29
F16-F19
1 amp
TB-A
F16
F17
F18
F19
One or up to four Customer Power Supplies. When less than four power supplies are used the customer may jumper the appropriate "load side" terminals of TB-A (i.e. plus load terminals 2 to 3, 5 to 6, 8 to 9 and minus load terminals 12 to 13 to 14 to 15).
Customer
DC Power
Supply
Customer
DC Power
Supply
System DC Ground

The voltage and current specifications are:

1. Rate: 500,000 (16 bit) words per second (maximum)

2. Output Voltage: Binary "1" = -3 v nominal

   Binary "0" = 0 v nominal

3. Output Current: 32 ma maximum (including termination and customer load).

4. Load Characteristic: Termination to customer +3 v and load must present 100 ohms characteristic to the transmission line. Customer +3 v must be between +2.88 and +3.4 v referenced to 1800 system dc ground.

5. Terminal Description: Register outputs terminate in a customer access area at the rear of the 1801 processor-controller.

6. Circuit Description: See Figure 2.5.

7. Line Length: 100 feet (maximum).

8. Line Capacitance: 18 picofarads/foot (maximum).

9. Wiring Practice: Use twisted pair conductors for wiring to the terminals in order to minimize pickup of electrical noise. This cable should not be run in the same cable with analog or digital inputs.

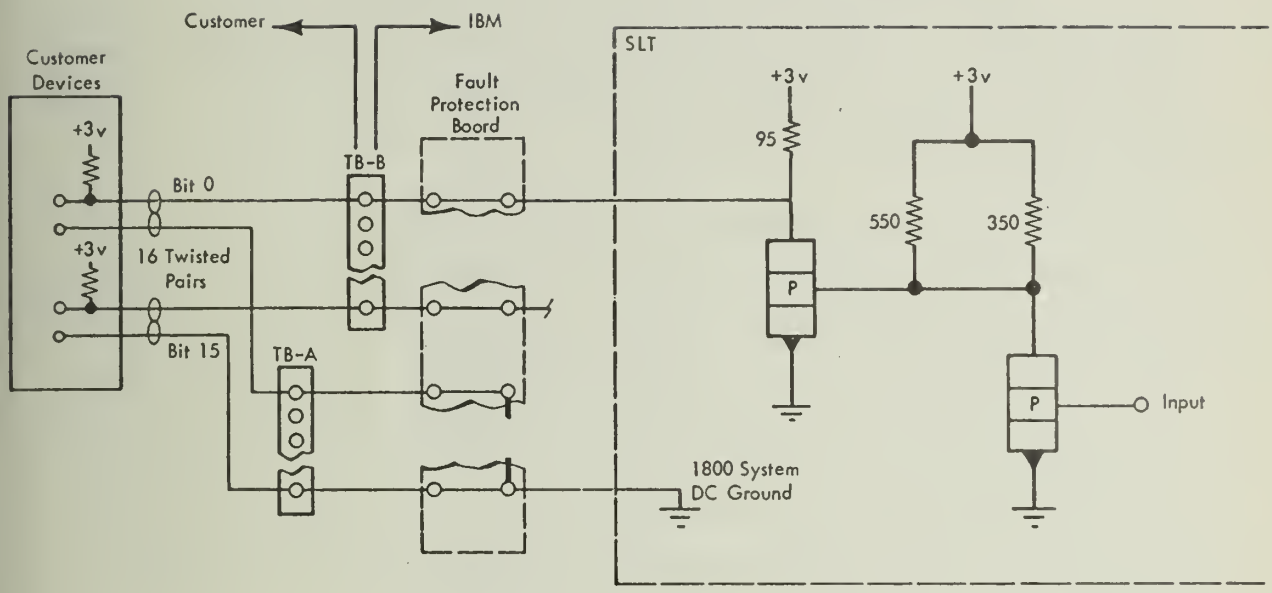


Figure 2.5. Register Output

2.4.5. Analog Input

The Analog Input units and features provide modular packaged equipment used to convert voltage or current signals to digital values. The modules used to accomplish the conversions include analog-to-digital converters, multiplexors, amplifiers, and other signal conditioning equipment.

A physical phenomenon is first sensed and converted to an analog electrical signal by sensors or transducers, such as thermocouples or strain gages. Electrical signals from sensors or transducers may be in the millivolt, volt, or milliampere range. Low voltage signals (less than 1 volt) must be amplified to a level acceptable for conversion to digital form. All customer lines from transducers are terminated at the control system on screw-down terminals. The signals are also conditioned at the terminals, including the filtering of extraneous signals, known as noise.

Conversion of analog signals from a voltage level to digital information is accomplished by an Analog-to-Digital Converter (ADC). Such converters, however, are complex enough so that if multiple sources of analog signals are to be converted, they share the use of one ADC. The switching is accomplished by a multiplexor. The data path from sensor or transducer to processor is shown by Figure 2.6.

The units and features that accomplish the analog input function are briefly introduced below, followed by more detailed descriptions.

As shown in Figure 2.6, customer input signals are routed through termination, signal conditioning elements, multiplexor switches, an amplifier (low level signals only), and into the analog-to-digital converter (ADC). The output of the ADC is presented to the processor-controller (PC) via the data channel from the ADC output register.

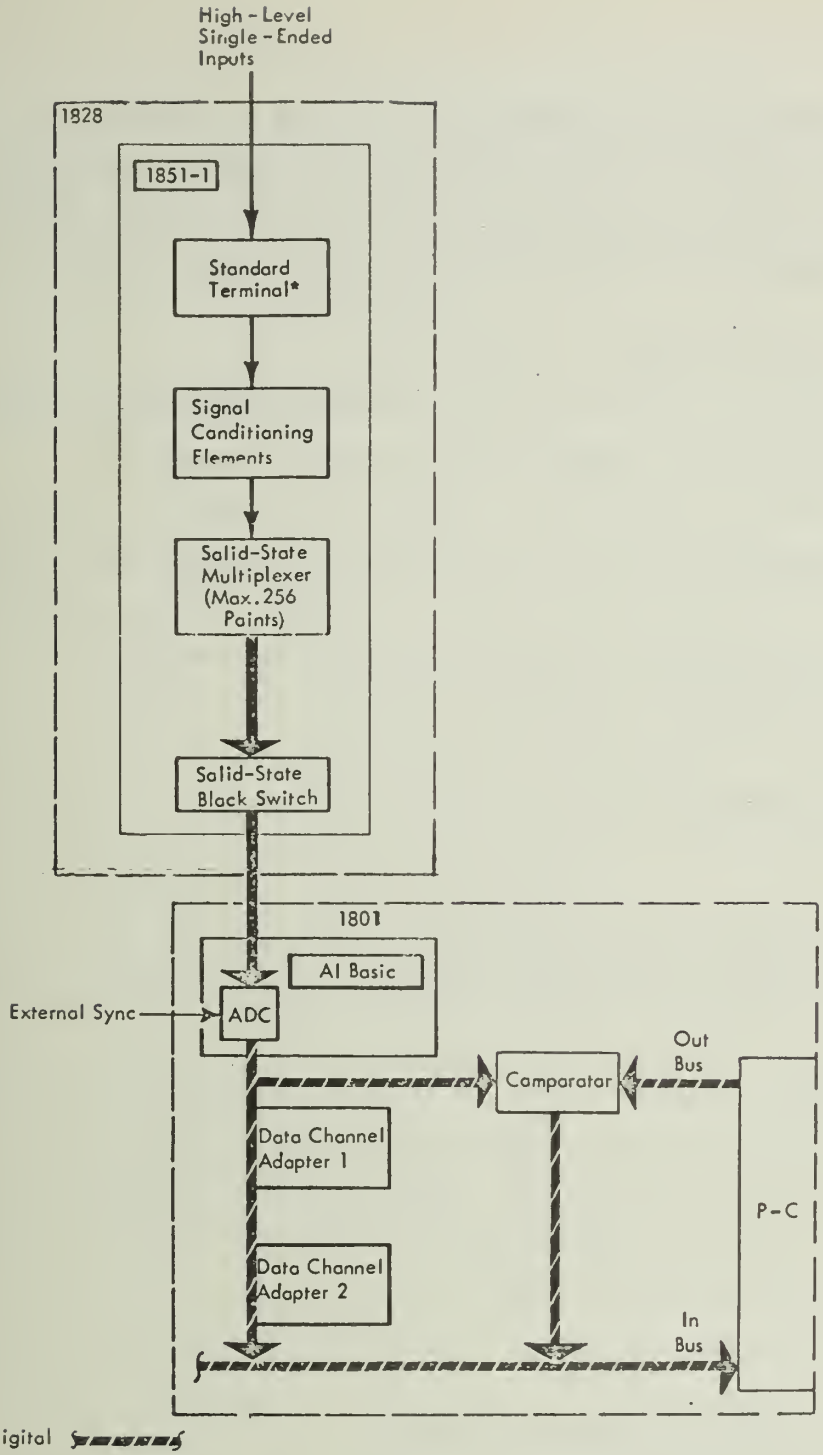


Figure 2.6. Interconnection of Analog Input Features

1851 Multiplexor Terminal-Model 1: A modular chassis which mounts in an 1828 Model 2 enclosure; up to 64 analog input multiplexor points (2 wire), signal conditioning elements for each point, and up to two differential amplifiers can be mounted in each terminal.

Multiplexor/S (HLSE): A solid state, high-level single-ended (HLSE) multiplexor to provide high-speed switching of analog input signals to allow use of a common analog-to-digital converter.

ADC-Model 2: Converts analog signals (±5 volt range) to digital values (8, 11, or 14 bits plus sign). It contains a Sample and Hold Amplifier for increased system conversion rates. The nominal system conversion rate is 20 kHz for this model.

AI Data Channel Adapter-1: Allows chained sequential mode of analog input (AI) operation by connecting a data channel to the analog input interface.

AI Data Channel Adapter-2: Allows random mode of analog input operation by connecting a second data channel to the analog input interface.

Comparator: Performs range checking on digital values developed by the ADC. The high and low limits are selectively obtained from the PC for those values to be checked. When values are determined to be out-of-limit an interrupt informs the PC. Only one PC cycle is required for each value to be limit checked.

2.4.5.1. 1851 Multiplexor Terminal

The 1851 Multiplexor Terminal is a modular chassis in which multiplexing and signal conditioning features can be mounted. The 1851 terminals are mounted in an 1828 enclosure. Up to 16 terminals can be included for any one ADC in a system.

The Model 1 Multiplexor provides for the insertion of up to 64 multiplexor points in groups of 16 points. Customer wires are terminated on screw down terminals. The matching elements are available for each multiplexor terminal. Up to two differential amplifiers can also be mounted in each terminal.

2.4.5.2. Multiplexor/S (HLSE)

The Multiplexor/S feature provides for solid-state multiplexing of high-level, single-ended (HLSE) analog inputs. System speeds are dependent upon the ADC, amplifier, etc., used in any particular system. See Figure 2.7.

The input voltage range is ±5 volts full scale. A Sample and Hold Amplifier in the ADC Model 2 permits conversion rates to be as much as 20,000 conversions per second with about 12 microseconds sample time.

2.4.5.3. Analog-Digital Converter (ADC)

The ADC provides the 1800 with the ability to convert bipolar analog signals (±5 volt signal range) to digital values. Model 2 includes a sample and hold amplifier which provides for increased system speed of conversion.

The ADC conversion time depends only upon the number of bits of output that are to be developed. Conversion times are as follows: 8 bits, 28 μsec; 11 bits, 36 μsec; and 14 bits, 44 μsec. Therefore, ADC conversion rates are 23,000 to 35,000 conversions per second (not including amplifier settling time). The input impedance of the ADC Model 2 is 0.1 megohms.

The 1800 System conversion rates will vary from 9,000 to 24,000 samples per second (dependent upon equipment installed and mode of operation).

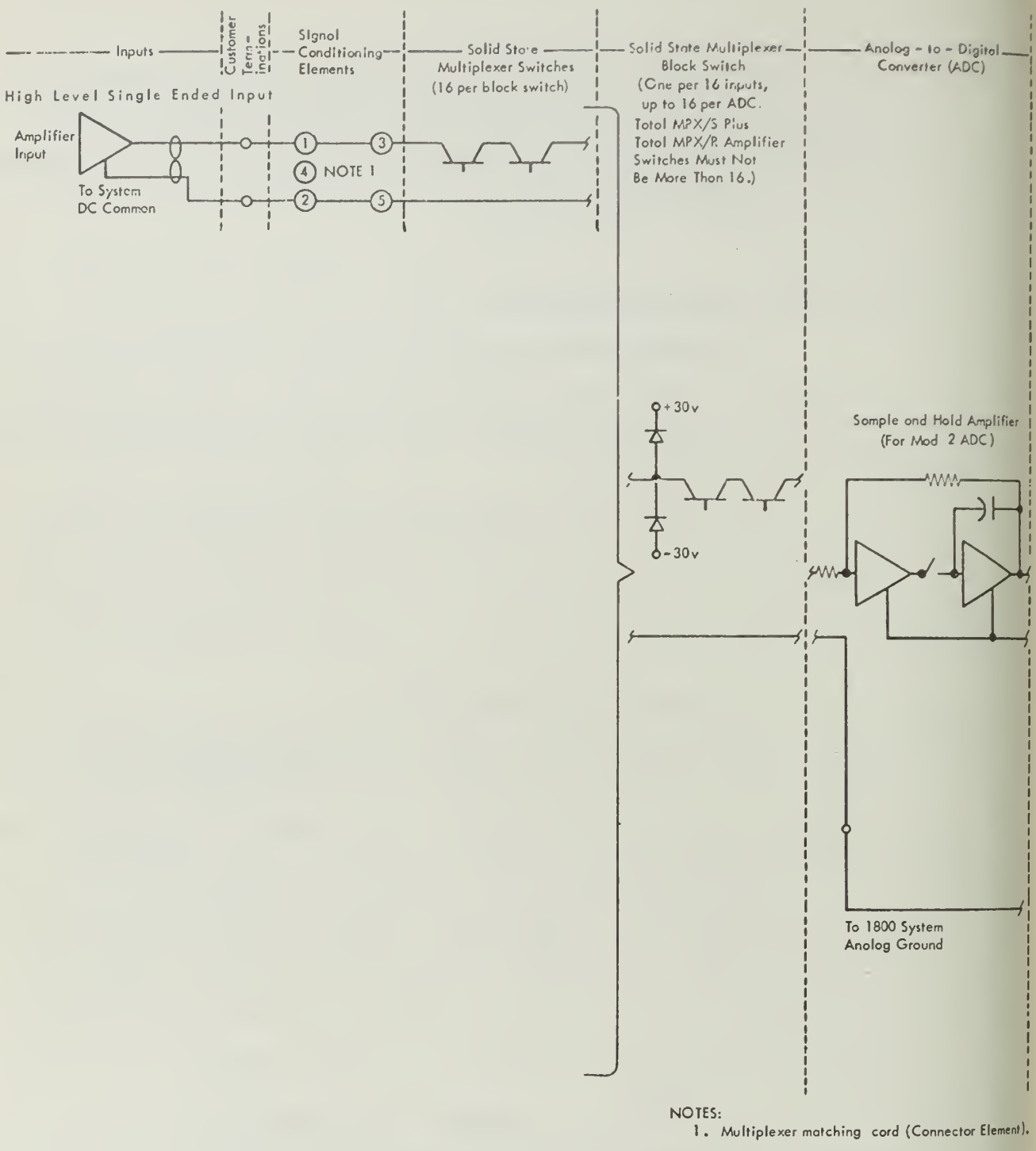


Figure 2.7. Solid State Multiplexor Inputs

2.4.5.4. Analog Input Calibration

The analog input calibration facility is housed in the 1828 Enclosure. Power is supplied to the calibration facility through the power switch on the front left side of the 1828.

The calibration facility provides the following dc reference voltages for calibration of AI features when the calibration facility is connected directly to an appropriate 1851 input terminal pair:

+5 volts	100 mv
-5 volts	50 mv
500 mv	20 mv
200 mv	10 mv

Exact voltages are measured at the factory and are recorded to five significant digits on the reference unit. Note that connections for +5 volt and -5 volt ranges are different.

A special high-level input point is selected by multiplexor address $13E8_{16}$ (which is outside the normal range of Mpx/S addresses) for ADC calibration only. The multiplexor calibration point can be addressed at any time by the customer program or diagnostic program for an operational check of the ADC. The reference voltage to be addressed is selected by changing connections on a terminal strip. An IBM Customer Engineer changes the connections on the terminal strip.

2.4.5.5. Sample-and-Hold Amplifier

The Sample-and-Hold Amplifier is an integral part of the Model 2 ADC. It is a single-ended amplifier capable of providing a short aperture time in the sampling of high-level analog signals and of providing a high accuracy hold function. The amplifier has an input impedance of 100K ohms. The program must consider the reversed polarities obtained from sample-and-hold input points.

2.4.5.6. External Sync

The operation of the ADC can be controlled by an external timing (sync) pulse. When the Solid-State Multiplexor is used, a "ready" condition is transmitted before the solid state switches are actuated. The external device provides a sync start pulse which allows the solid-state switches in the multiplexor to be actuated and then conversion of the selected signal begins.

An "8" bit in the modifier of a IOCC, either "Write" or "Initialize Read," sets up the external sync mode. The absence of an "8" bit in the modifier of either a "Write" or "Initialize Read" command terminates the external sync mode.

2.4.5.7. Comparator

The Comparator performs selective checking on the digital values converted by the ADC. A range type check is made to confirm that the converted values are within specified limits. The limits are obtained from the Multiplexor Address Table (one PC cycle delay allows both limits to be acquired) whenever a check is required. The PC is informed of an out-of limits condition by interrupt. The two Analog Input Data channel adapter features are a prerequisite to this feature.

In order that a range comparision can be made, both a high limit and a low limit must be set. In converting many analog input source signals, it may be necessary to monitor each signal to assure that the signal remains within specified bounds. Normally, a number of these signals are redundant and other signals need only be checked occasionally. To allow for flexibility of checking input signals, a separate control (in Multiplexor Address word) is added to instruct the Comparator to perform checking when required.

It should be noted that limit words need not remain static. For example, when a particular high limit is exceeded, then a single change will permit recognition of the return of the signal within the

former limits. The high limit is substituted for the low limit and the maximum value is set for the high limit. If the interval timer is read after each limit is exceeded, then the time interval that the signal was out-of-limits is known.

3. System Software

3.1. Operating System Requirements

The control program for the 1800 computer must meet several severe requirements. For example, consider an 1800 job which involves high-speed analog to digital conversion. Such a program will rely heavily on large input/output buffers, immediate response to interrupts, etc. In short, data will be entering and leaving the processor-controller (PC) at such a rate as to allow essentially no time for system overhead. Historically, such programs were written for stand-alone execution: the program was responsible for loading itself into core and performing all of its functions, including input/output, interrupt handling, etc. This method is obviously undesirable even on a stand-alone computer; the fact that the 1800 will be controlled by the System/360 makes such a configuration impossible.

The solution to these problems is an operating system which is passive in nature. For example, during execution of an 1800 job, the operating system can gain control from the problem program in the following ways only:

1) Detection of an abnormal condition (such as a protect error, etc.);
2) Operator intervention (via the console typewriter);
3) The job itself;
4) The System/360 computer.

If we assume that (2) is not an arbitrary action, then (4) becomes the only interrupt which could disrupt a job executing in a proper manner. We eliminate this problem by requiring that the System/360 communicate with the 1800 by request of the 1800 only, unless the System/360 has detected an abnormal condition which the 1800 does not have the ability to recognize. This called an "1800 master-360 slave" environment.

Other, more specific requirements and plans for attacking them are:

1) Available core storage. In order to take up the smallest possible amount of core, the resident portion of the operating system will include only those programs essential to the execution of all jobs. These programs will include interrupt handlers, System/360 communication routines, console supervisor, storage dump and program loader routines, input/output supervisor, etc. All other programs will be in the form of subroutines dynamically loaded with the user's program as requested. Such subroutines will consist of device-dependent I/O error recovery routines, data conversion programs, etc.

2) Interrupt processing. Some 1800 jobs will need to process their own interrupts. The resident operating system will allow user interrupt exits to a limited extent.

3) Operator communication. Operator/user control of a program will be available through the 1816 typewriter keyboard. The operating system will contain an extensive set of routines which will allow operator/program conversation in a flexible manner.

4) System/360 Model 75 communication. There will be two communication paths between the 1800 and the 360-75. The first of these is the pool of System/360 tape drives which will be attached to both systems. Secondly, two-way communication will be provided through the 360-50. The 1800-System/360-50 channel-to-channel adapter will appear to be a series of pseudo-tape units to the 1800 program. Data output to one of these pseudo-units will be read in by the 360-50 and stored on a direct-access device. The same concept applies to the 50-75 connection; therefore, a subsequent job on the 360-75 may "read" the pseudo-tape, in which case the 360-50 will extract the data from the direct-access device and send it to the 360-75.

5) SYSIN/SYSOUT facilities will be handled in the same manner as (4). When a user's job is read in by the 360-50, a series of pseudo-tapes is created on 360-50 disk storage for that job. One of these pseudo-tapes (the SYSIN tape) is then loaded with the card images which make up the job. The 1800 (or the 360-75) will process the job by issuing read requests to the 360-50 for data from the SYSIN file and write requests for data to the SYSOUT file. When execution of a job is completed, the 360-50 dumps the contents of the SYSOUT and SYSPUNCH files to a printer and punch, respectively. The other pseudo-tape files (there are sixteen in all) may be used for 1800-360-75 communication, scratch, etc. See Figure 3.1.

3.2. Operating System Components

1) Input/Output Supervisor (IOSUP). The function of this program is to schedule system or user requests for I/O to devices other than the console typewriter. Logic consists of verifying the availability of the I/O device, initiating the I/O, and, if necessary, recovering from an initial failure such as device out-of-ready status. Once the I/O operation is initiated, IOSUP returns control to the calling program (in most cases a system I/O subroutine which was invoked directly by the user program). Input to the I/O supervisor consists of a device address, I/O control command to be executed, and an event control word (ECW

2) Console I/O Supervisor (CNSUP). CNSUP controls all input from and output to the 1816 typewriter console. Messages input by the operator are converted to EBCDIC and passed to CSERV for appropriate action. Output of program-generated messages to the operator is initiated by CNSUP.

3) Console service program (CSERV). Operator messages input to CNSUP are routed here for action. CSERV may take such action as canceling a job, passing a response on to a user program, etc.

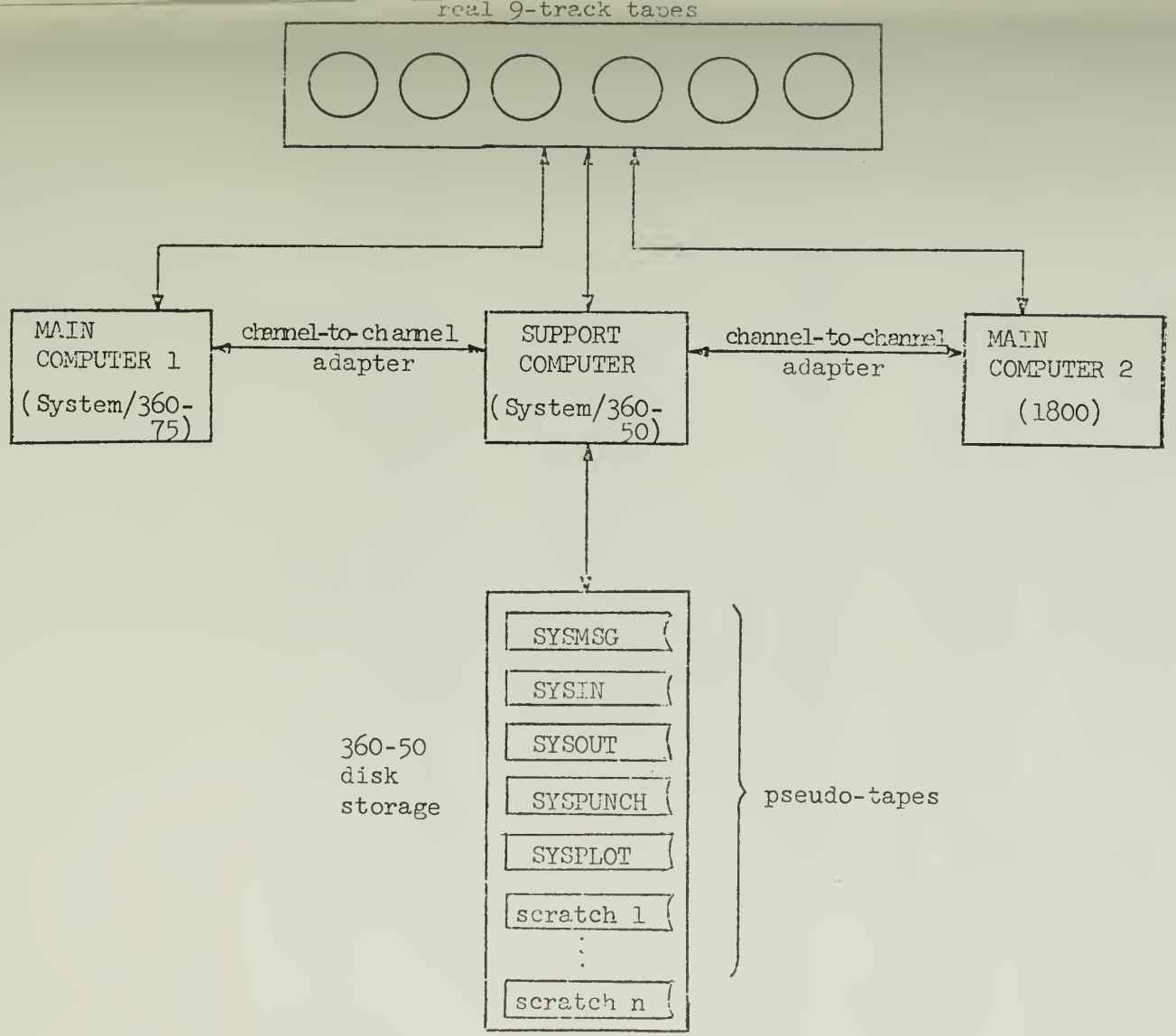


Figure 3.1.

Communication Between Central Computers

4) Dump program (DUMP). The DUMP program, upon request, takes panel, partial core, or full core dumps. Although normally invoked by the system upon detection of an abnormal condition, DUMP may also be called by a user program for snapshot (debugging) purposes.

5) System Loader (LOADR). LOADR reads in user programs and subroutines, relocates them into user core, resolves external references, prints a storage map, etc. Although normally called by the Job Scheduler, future plans for LOADR include dynamic reference by the user for overlay or "ping-pong" purposes.

6) Time supervisor (TIME). Currently, the TIME supervisor provides the caller with the current time of day. Future plans call for interval timing logic.

7) Channel-to-Channel Adapter Supervisor (CASUP). CASUP controls all communication from the Support Processor (System/360-50) via the channel-to-channel adapter.

8) Job scheduler (JBSCH). This program schedules jobs for execution by interpreting control cards, allocating I/O devices, etc. JBSCH resides in the user portion of core as a transient module, i.e., it is overlaid by user programs.

9) Subroutine library. An extensive set of subroutines will reside on Support Processor direct-access storage. References to these routines by a user program (via CALL macro) will result in their being loaded with the user program by LOADR.

3.3. Interrupt Logic

In keeping with the prerequisite of simplicity with flexibility, the interrupt logic is designed as follows: All processes asynchronous to the CPU (such as interval timing, I/O operations, etc.) will signify their termination by interrupt. The interrupt portion of the operating system will then store the status of the completed event into the associated event control word (ECW), thus changing it from zero to non-zero.

For example, when the I/O supervisor (IOSUP) initiates an operation to the 1442 card reader, the address of a zeroed ECW will be placed into a location which can be referenced by the interrupt supervisor. Control will then return to the calling program, which may proceed with main line computing or wait for completion of the I/O operation. The latter is accomplished by calling the WAIT routine, passing to it (as an argument) the address of the ECW associated with the event being waited for.

Upon completion of the I/O operation, an interrupt will occur. The interrupt supervisor will decode it, placing all status information into the ECW (thus setting it non-zero). Control will then be returned to main-line execution, which may be the WAIT routine. WAIT will ascertain that the ECW is now non-zero and will therefore return to the calling program. The program will then process the data in the ECW as post-operation device status by checking for I/O errors, etc. Note that IOSUP and WAIT may be called directly by a user program; however, the typical mode of operation will be to call a system subroutine which will in turn perform the detailed work. See Figure 3.2.

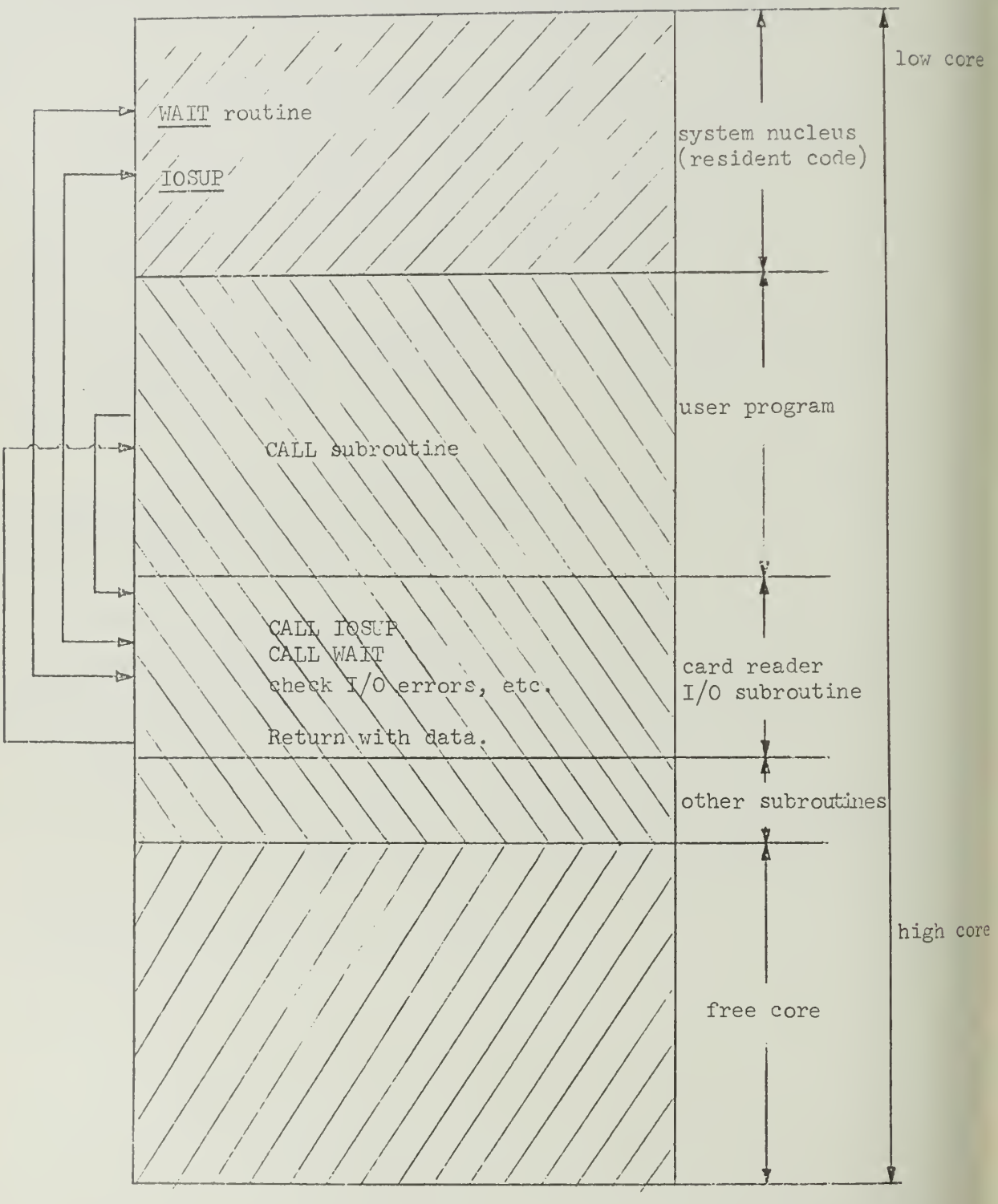


Figure 3.2.

I/O Subroutine Flow of Control

3.4. Languages

At the current time, the 1800 programmer has one language at his disposal - 1800 assembler language. Furthermore, the 1800 assembler is a System/360 program. The fact that the two computers may easily communicate with each other makes this situation an advantageous one, however, since the 1800 is not a good computer for compilers and assemblers (no character manipulation or translate instructions, for example).

The lack of such a language as FORTRAN is not too critical when one considers that the System/360-75 is much more suitable for numerical computations than the 1800. Besides being an order of magnitude slower, the 1800 has no floating point hardware.

The Department is considering implementation of a higher level language in the future.